REMARKS

The indication of allowable subject matter in claims 3, 5 and 6 is acknowledged and appreciated. The amendment to the claims is directed solely to eliminate "means" language, improve syntax and provide consistency among the claims; and is not being made to obviate any pending rejection in the outstanding Office Action. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 1, 2 and 4 stand rejected under 35 U.S.C. § 102 as being anticipated by Matsuda et al. '533 ("Matsuda"), and claim 7 stands rejected under 35 U.S.C. § 103 over Matsuda in view of Applicant's admitted prior art. Claims 1 and 7 are independent. These rejections are respectfully traversed for the following reasons.

Each of claims 1 and 7 recite in pertinent part, "a hold over unit for outputting hold over data used for performing phase correction; a second selector for selecting and outputting one of the phase correction data supplied from said comparator and the hold over data supplied from said hold over unit." The Examiner apparently relies on hold over circuit 63 shown in Figure 1 of Matsuda as both the claimed "hold over unit" and the claimed "second selector." It is respectfully submitted that this interpretation is *per se* improper because the Examiner has effectively read a *single* element from the prior art (hold over circuit 63) as *two* elements from the claimed invention ("hold over unit" and "second selector"). The Examiner has apparently attempted this improper claim interpretation on an alleged similarity in functionality and operation between the present invention and Matsuda.

However, it is respectfully submitted that the express claim language precludes such a broad interpretation. For example, the claimed second selector can select and output one of the phase correction data ***supplied from said comparator*** and the hold over data ***supplied from said hold over***

unit. In other words, the claimed second selector receives data from two sources (e.g., one exemplary embodiment is shown in Figure 1 of Applicants' drawings, whereby comparator 2 and hold over unit 3 each can output data to the selector 4).

In contrast, the hold over circuit 63 of Matsuda is arranged so as to receive a *data* signal from only the comparator 61 and functions to either hold the data momentarily and output it to the VCO 64 or lock its output at the previously received voltage (*see* col. 2, lines 27-29 and lines 37-44). The Examiner alleges that the "hold over circuit [63] acts as a selector for outputting the phase corrected data or outputs a hold over signal." However, the alleged selection of Matsuda is NOT a selection between the outputs of two sources but rather is a selection between *operational modes* of the hold over circuit 63 itself. That is, the hold over circuit 63 of Matsuda, at best, switches between a hold and release mode in stable conditions, and a voltage-lock mode in unstable conditions whereby the hold over circuit operates to lock its previous voltage output.

Because of this structural arrangement of Matsuda, the hold over circuit 63 must be configured to include circuitry enabling the voltage-lock of a previously outputted voltage. Moreover, even during stable operation, the phase correction data of Matsuda necessarily must flow through the hold over circuit 63 so as to be held for a moment (*see* col. 2, lines 27-29), thereby introducing recurring delay. Whereas, as exemplarily shown in Figure 1 of Applicants' drawings, the present invention can provide the capability for the phase correction data to bypass the hold over unit 3 during stable operation.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986),

based on the forgoing, it is submitted that Matsuda does not anticipate claim 1, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 7 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102 and 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are

any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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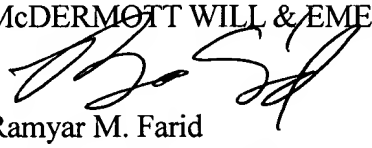

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